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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53 (c).

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TITLE OF THE INVENTION (280 characters max)

AN ANALOG FRONT END (AFE) CIRCUIT THAT IMPROVES ECHO REJECTION IN COMMUNICATIONS SYSTEMS

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ENCLOSED APPLICATION PARTS *(check all that apply)*

☒ Specification *Number of Pages* 7
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☐ Application Data Sheet. See 37 CFR 1.76
☐ CD(s), Number
☐ Other (specify)

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT *(check one)*

☐ Applicant claims small entity status. See 37 CFR 1.27.
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☒ No
☐ Yes, the name of the U.S. Government agency and the Government contract number are:

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Date 06/07/2002
REGISTRATION NO. *(if appropriate)* 46,145
Docket Number: 1340P087Z

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

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PROVISIONAL PATENT

UNITED STATES PROVISIONAL PATENT APPLICATION

FOR

AN ANALOG FRONT END (AFE) CIRCUIT THAT IMPROVES ECHO REJECTION IN COMMUNICATIONS SYSTEMS

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1. Problem Statement

One of the main impediments to increasing the performance of a duplex DSL modem is the effect of the residual signalfrom the transmitter that is present at the receiver, i.e., echo. Although most analog front-end circuitry does cancel some amount of echo (typically 13-20 dB), greater echo cancellation (approximately 30 dB) is needed in order that the various sources of noise in the receiver are minimized, especially for loop lengths in excess of 6000 feet.

2. Proposed Solution

Most standard designs for DSL modems incorporate the half-bridge circuit depicted in Figure 1. The circuit is depicted in a single ended mode for simplicity; most circuits used in actual modems are fully differential. The data to be transmitted is converted from a digital signal to an analog signal by the transmit DAC and line

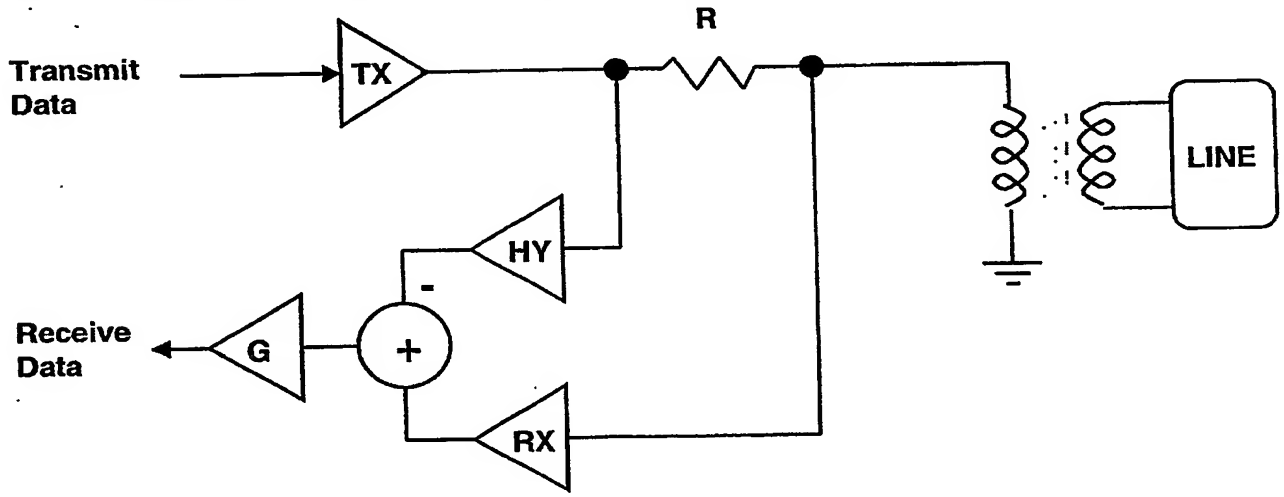

Figure 1: Standard Analog Front End for DSL Modems

driver [TX], dropped over a drive resistor with resistance R, and coupled to the line via a transformer. The echo is reduced by measuring the transmitted signal by a hybrid input [HY] and the signal at the transformer by a receive input [RX], and composing the received signal as some linear combination of both. Typically, the gain on the HY input may be adjusted within a small range about unity, while the RX input has unity gain. In the diagram above (Figure 1), it is clear that if the impedance of the line as seen through the transformer is equal to the resistance of the drive resistor, and the HY input gain is ½, then the component of the transmitted signal in the received signal is completely eliminated. Unfortunately, the impedance of the line as seen through the transformer is not only not resistive, but also has an impedance that is a complex function of frequency. Thus, it is quite difficult to assure that the signals being subtracted at the summing junction are similar (both in gain and in phase). Thus, the typical reduction of the transmitted signal component in the received signal is about 13-20 dB.

The central problem to echo cancellation is to design an AFE circuit such that the inputs to the HY input and RX input are similar in gain *and phase*. Three elements were absolutely critical for the design solution discussed in this document. These are:

1. The ability to model the entire circuit along with transmission line with high accuracy, and
2. An understanding of the theoretical framework that relates gain and phase in a complex circuit, specifically the relationship between gain and phase in a nonminimum phase transfer function, and
3. An understanding of the conditions under which parallel transfer functions add to form an equivalent nonminimum phase transfer function.

The problem of modeling the discrete components in AFE circuitry is fairly straightforward. This is usually in a SPICE environment; however, without a good two-port model of a transmission line, SPICE modeling is useless. Fortunately, good analytical two-port models of transmission lines exist [1], and are expressed in a format:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}. \tag{1}$$

Unfortunately, this format is not readily adapted to SPICE. Nevertheless, with some elementary linear algebraic formulae, this may be converted to the format:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} E & F \\ G & H \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \tag{2}$$

which can be implemented as a circuit using standard "E" blocks with SPICE [2]. These blocks accept as an input voltages and output current with some inherent gain. Since the resulting variables E, F, G, and H are frequency dependent, the "E" block must include a lookup table that describes the complex gain as a function of frequency with sufficient resolution. A MATLAB script was written which completely transformed the analytical two-port model in (1) into a SPICE library script that could be imported into SPICE as an integral circuit block.

Armed with an accurate transmission line model, the task of designing an AFE circuit with high echo rejection becomes possible. The Voyan Technology design starts with a reference design provided by Silicon Laboratories (Figure 2), which is essentially the prebalance circuit found in [3], but with an additional first order high pass filter stage at both the HY and RX inputs on the Silicon Laboratory Si3101 chip and with the signal from the line provided by a separate coil on the transformer. One problem with this reference design is that while the prebalance circuit reduces the component of the transmitted signal to the RX input, it can decrease the damping of the circuit and even change the transfer function from the TX output to the RX input to a non-minimum phase function [4]. While the first effect is troublesome, the second is disastrous. To eliminate this problem, the polarity of the connection between the TX outputs and RX coil inputs were reversed (purple change, Figure 3). This ensured that the transfer function from the TX output to the RX input was minimum phase. Also, by varying the ratio of R_3 to R_4 and R_5 to R_6 an appropriate amount of damping of the transfer function could be maintained. Without an appropriate amount of damping, a more reactive circuit to the HY inputs would be required, which in turn would require inductors as well as capacitors and resistors to affect the appropriate gain/phase matching at the RX and HY inputs. This, however, would greatly increase the complication of the circuit, as well as adding possible nonlinearities in the circuit due to the nonlinearities of the inductors.

Even though the polarity of the prebalance circuit was modified to increase the damping of the circuit, the resonance could not be entirely eliminated. Thus, the circuit appears to have a slightly undamped roll-up at low frequencies (below the corner frequency of the high pass filter to the RX inputs). The effect of this is to retard the phase more sharply at RX inputs than the HY inputs at low frequencies, since the HY inputs have only a first order rollup. This in turn mismatches the phases at the two inputs at these frequencies, which is a

consequence of Bode's Integral of Phase. This law describes the relationship between the gain slope (*dG/du*) the phase ϕ of a nonminimum phase transfer function [5]:

$$\phi(\varpi) = \frac{1}{\pi}\int_{-\infty}^{\infty} \frac{dG}{du} \ln\coth\frac{|u|}{2} du \quad , \tag{3}$$

where $u = \ln(\omega/\varpi)$. This retardation of the phase has a deleterious effect on echo cancellation near the corner frequency of the high pass filters at the HY and RX inputs of the AFE chip. To mitigate this problem, the high pass filter circuit at the RX inputs was enhanced to include two parallel passes, one with just a capacitor and one with a capacitor in series with a resistor (red additions, Figure 3). This latter element shapes the gain slope of the roll-up of the TX to RX transfer function so that it rises more slowly, ensuring that the phases at the HY and RX inputs are more closely matched at low frequencies. This feature is responsible for

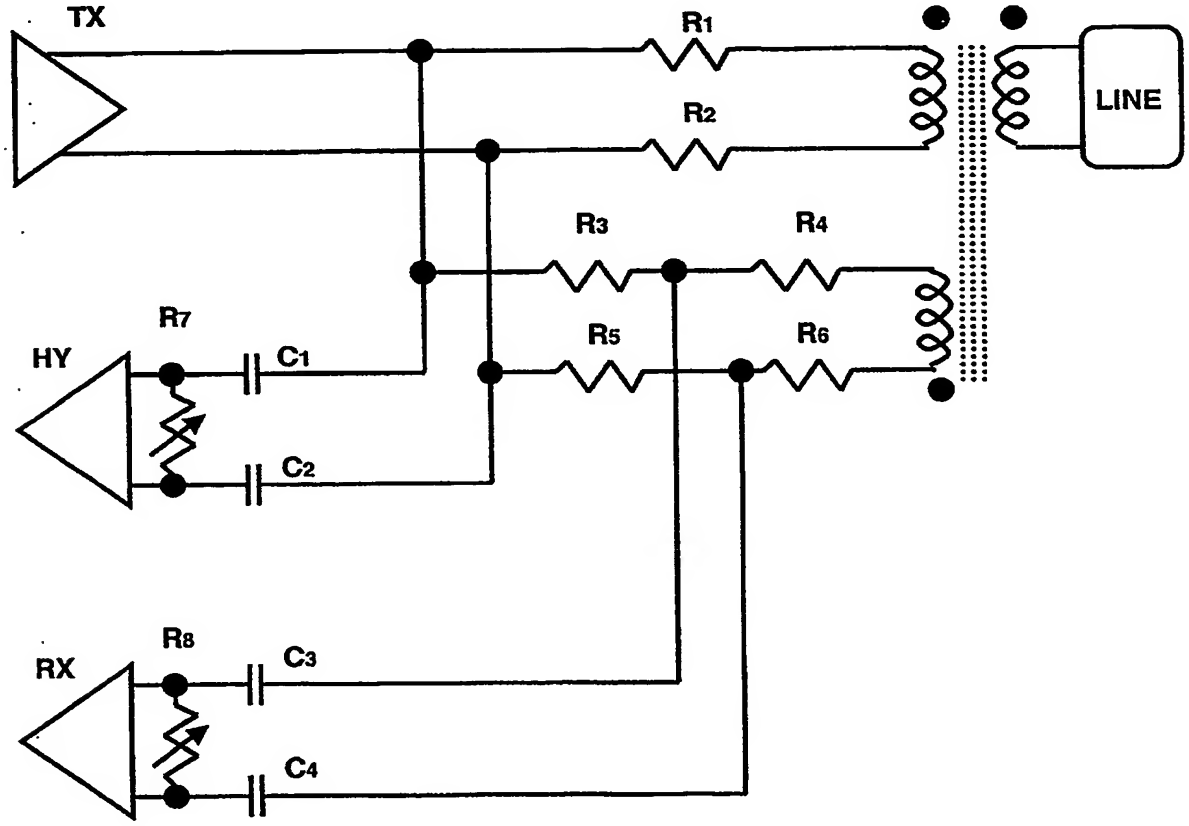

Figure 2: Silicon Laboratory AFE Reference Design

a 10 dB increase in the echo rejection at lower frequencies.

An additional impediment to good echo cancellation arises from the effect of the leakage inductance of the transformer. This has the effect of increasing the effective impedance of transformer, thereby lifting the gain slope TX to RX transfer function slightly at high frequencies (around 350 kHz and above). This small slope differential causes a phase mismatch at the HY and RX inputs of the AFE chip at these frequencies. To mitigate this problem, HY input was enhanced to include two parallel passes, both with a capacitor in series with a resistor (blue additions, Figure 3). These elements causes the gain slope of the TX to HY transfer function to rise in a similar fashion to the TX to RX transfer function, ensuring that the phases at the HY and

RX inputs are more closely matched at high frequencies. This feature is responsible for a 10 dB increase in the echo rejection at these frequencies.

As a result of these modifications, the circuit design in Figure 3 achieves an echo rejection performance that is about 30 dB for 26 AWG copper loops with no bridged taps, which significantly improves the state of the art for AFE design.

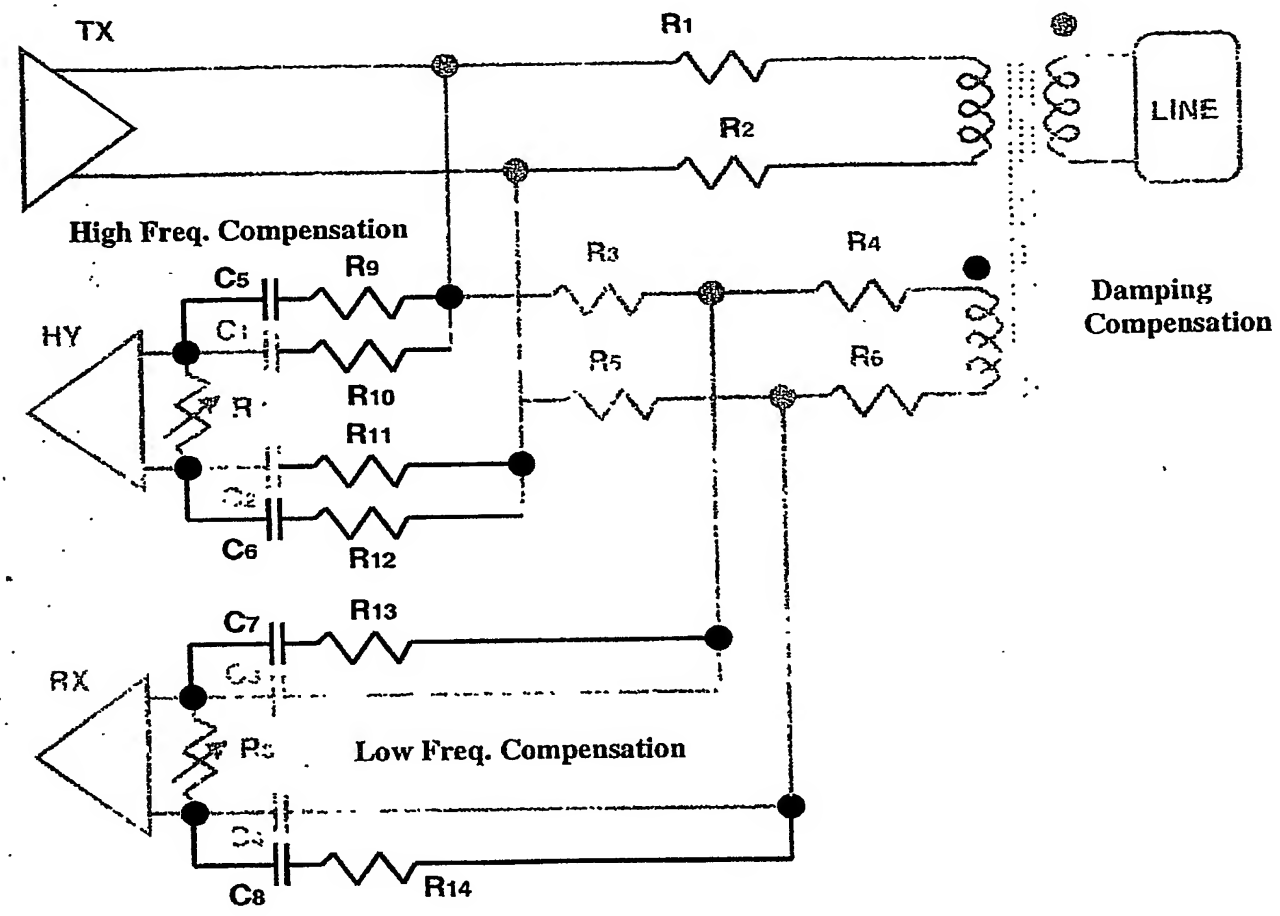

Figure 3: Voyan Technology AFE Design

Appendix

Circuit Element	SiLabs Reference Design	Voyan Technology Reference Design
R_1, R_2	3.3 Ω	2.4 Ω
R_3, R_5	200 Ω	200 Ω
R_4, R_6	100 Ω	50 Ω
R_7, R_8	Variable 300-6000 Ω	Variable 300-6000 Ω
R_9, R_{12}	N/A	1 Ω
R_{10}, R_{11}	N/A (0 Ω)	60 Ω
R_{13}, R_{14}	N/A	4.99 kΩ
C_1, C_2	2.2 nF	3.3 nF
C_3, C_4	2.2 nF	3.9 nF
C_5, C_6	N/A	470 pF
C_7, C_8	N/A	18 nF

ABSTRACT

An Analog Front End (AFE) circuit with increased echo rejection performance.